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Finding Solutions to the Challenges in Package Interconnect Reliability

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Finding Solutions to the Challenges in Package Interconnect Reliability

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ABSTRACT

The microelectronic industry has continuously driven for greater integration of functionality and capability. This has led to some significant challenges for the industry. For example, to improve electrical performance, materials with low dielectric constants are being added to the silicon structures. These fragile materials in silicon interconnect layers present a significant challenge to the development of reliable package assembly processes. Similarly, the introduction of new features has led to the need for smaller, weaker interconnects between the package and the system board.

Recently, these trends have been coupled with changes to the operating environment for electronic devices. With the growing trend toward mobile computing, the risk of interconnect damage from devices being dropped has grown. This is further complicated by the legal requirement to remove lead-containing materials from the package. This requirement affects the package interconnects by eliminating solder materials that have been traditionally used, whose behavior is well understood and quantified.

The traditional approach to resolving such challenges involves finding solutions through large designed experiments to optimize the design, material, and process choices. These methods have met with difficulty due to the complexity and interdependency of the issues. In this paper we look at the application of new engineering mechanics tools and methods to better understand the fundamentals of package reliability. To determine the reliability, one must be able to assess both sides of the reliability equation: the stress imposed by the loading condition and the material strength. In general, if the strength of the interconnect exceeds the stress applied throughout the life of the package, then it will be reliable. While it is not always possible to accurately predict and quantify both sides, the techniques discussed can help engineers make better judgments and can provide direction to technology development.

In this paper we describe three case studies using the approach described above. The first case study describes how bump pull/shear metrologies are used to understand the impact of various assembly and silicon fabrication processes on the silicon interconnect strength. The second case study provides a thorough analysis of second-level interconnect reliability (BGA) under shock loading conditions in laptops. The last case study shows how these measures can be used to enhance the material selection process in selecting a second-generation lead-free solder material. This approach has lead to the successful launch of lead-free package technologies with higher density interconnects.

INTRODUCTION

Classically, the interconnects of the package are defined as first level and second level. The first level connects the silicon die to the package. This may be a wirebond or flip-chip-type interconnect. The second level is the connection between the package and system board. In our case, the second level is a ball grid array.

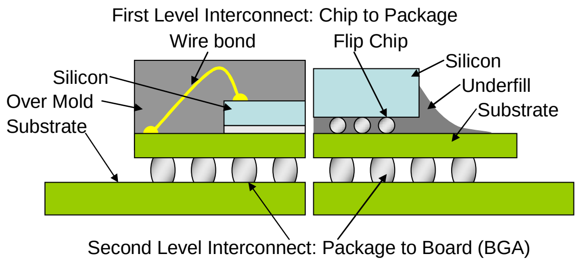

Figure 1: Interconnect definition for flip chip and wire bond packages

First-Level Interconnect

Presently, the reliability of the first-level interconnect is being challenged by two changes: low dielectric constant (low k) materials and the need to remove lead materials from the package. In order to reduce electrical signal delays and improve the performance of the silicon circuits, the industry in general has shifted toward reduced k material for the inter-layer dielectric in the silicon die. These materials challenge the mechanical reliability since they are substantially weaker than previous materials. This is further compounded by the legislative requirement to remove lead from the package. At present all of the available lead-free materials have unfavorable properties that impose additional stress on the first-level interconnect.

Second-Level Interconnect

At the second-level interconnect there is a distinct set of challenges. The first challenge is that mobile computing is rapidly increasing in popularity, with both laptops and smart phone/PDAs. As people carry these devices around more frequently they will also drop them more often. This imposes more stringent shock conditions on mobile components.

The second challenge arises from the need to switch to lead-free solders. SAC405/305 alloy, the current industry-standard second-level interconnect solution, is significantly worse than eutectic SnPb alloy in terms of its shock performance, as much as 40% lower as compared with eutectic SnPb. SAC405/305 alloys with their inherently low shock resistance are not optimal for next-generation, lead-free applications in mobile computing.

The third challenge is that long-term industry trends drive for greater integration of functions and features in devices. This implies that a greater number of interconnects are required to facilitate these new features. Mobile computing also exerts down pressure on device size. These two trends combine to constantly reduce the size of the second-level interconnect, thus making each individual interconnect weaker.

To meet the challenges of both the first-level and second-level interconnects, new approaches are needed that will expand our knowledge and allow cost-effective solutions while maintaining the pace of technology development.

APPROACH

The microelectronic industry has a very short development cycle time. At this frenetic pace there is a strong temptation to take a "build and test" approach. This typically takes the form of a designed experiment with multiple design, material, and process settings. All of these test legs are then tested through conventional reliability tests. Should any of the experiment legs pass the reliability test then the new process or material is accepted. This method works well for establishing process parameters when the variable space is limited and reasonably well understood. That said, the method often fails when the converse is true. In those cases where it does succeed it is difficult to typically extrapolate toward future developments since the DOE is not based on an understanding of fundamental material properties.

We propose using metrics related to fundamentals of stress and material strength to enhance our understanding of these material properties. This approach seeks to answer the question "What are the characteristics of the optimal solution?" By characterizing the stress being applied and the corresponding strength, one can gain much better insight into the fundamental cause of the reliability issue as well as solving the problem of the day.

Three case studies follow to illustrate this approach to solving technical problems in package interconnects. Each study either measures the strength or stress related to an interconnect reliability issue.

CASE 1: MEASUREMENT OF EFFECTIVE SILICON BACKEND STRENGTH USING BUMP PULL/SHEAR TECHNIQUES

The integration of highly fragile low-K Inner Layer Dielectric (ILD) materials is critical to the reduction of signal propagation delays, which stem from continued geometric scaling of integrated circuits [1]. As a result, the silicon backend (passivation layer, low-K ILD, silicon oxide layers) is prone to early failures if the applied thermomechanical stresses exceed the effective strength of the stack up. The Coefficient of Thermal Expansion (CTE) mismatch between silicon and the package substrate, along with the high stiffness of lead-free (Pb-free) interconnects, are the primary source of thermomechanical stresses. The problem is further exacerbated by reliability tests, such as the Highly Accelerated Stress Test (HAST) or temperature cycle,

which are necessary to ascertain the life of these ILDs under "real life" conditions [2].

Problem Statement

With increased mechanical and material complexities and shorter time to market, the traditional brute force build and test approach has proven to be costly and inefficient. In order to accurately assess the mechanical reliability of a package design, one must be able to quantify both sides of the reliability equation, the applied stress versus the intrinsic strength of critical package structures. In general, if the strength exceeds the applied stress throughout the expected lifetime of the product, then it will be reliable. In order to influence the product design and development cycle in a timely manner, it is essential to implement Quick Turn Metrologies (QTM) which generate material strength comparisons of the die backend and provide direct feedback to the manufacturing process. The availability of 1st wafer-level bump pull and bump shear bond strength testing techniques, using commercially available tools, serves the industry extremely well in this regard.

Metrology Selection

Commercially available bond strength testers are capable of conducting shear and tensile tests of wafer-level bumps. Bump shear tests are carried out using a 1-mil wide (25.4um) stylus. Bump pull tests are conducted using a 100um tweezer jaw with a 1Kg range pull cartridge. In both cases, the peak force to failure is reported. Results of strength measurements are also coupled with failure analysis methods such as Focused Ion Beam (FIB) for sample preparation, with subsequent Scanning Electron Microscopy (SEM) and Energy Dispersive X-ray (EDX) analysis in order to validate resulting failure mechanisms. Figure 2 shows the details of each experimental setup.

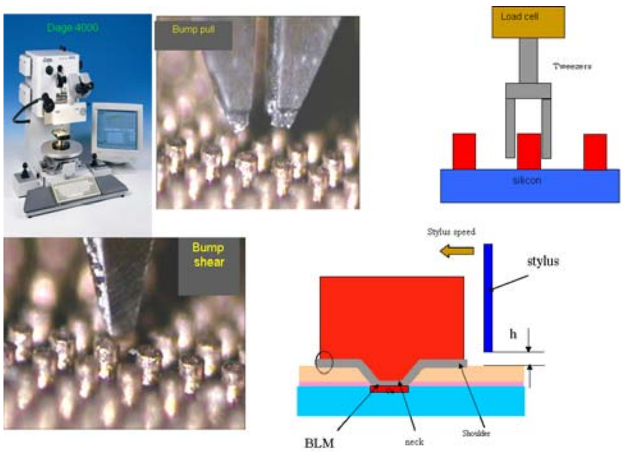

Figure 2: Bump pull and shear experimental setup showing the tool, and the schematic representation of how shear/pull events are executed

The experimental procedure involves clamping the die through the use of a suitable sample stage and selection of appropriate tool settings such as test speed, stylus height for bump shear, and tweezer grip pressure for bump pull. The bump pull and shear techniques may be applied to testing either on singulated silicon die samples post FAB wafer assembly processes, or on dies that were first assembled on a package substrate and subsequently removed by heating the package. The latter process is used to understand the impact of assembly-related parameters on silicon backend strength.

Results

Application of Bump Shear to Evaluate the Impact of Flux Exposure on ILD Strength

One critical challenge faced during development of 90nm technology involved the impact of the C4 assembly processes on the ILD stack-up. One case in particular involved the interaction of a particular flux used in the chip attach assembly step, which exhibited a strong correlation to ILD fracture following chip join, as revealed by acoustic scan "white bump" signatures represented in Figure 3(a).

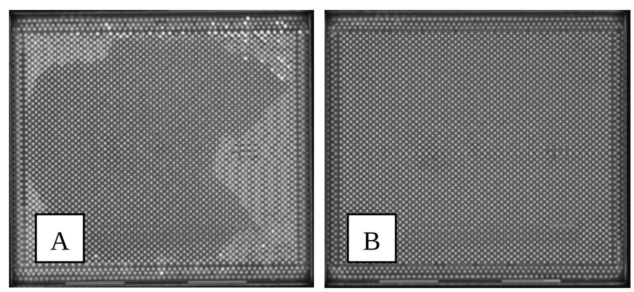

Figure 3: Acoustic scan white bump count resulting from die-flux interactions

Image A reveals a white bump ILD crack signature resulting from an interaction with the problematic flux. Image B shows no white bump count resulting from a different flux material. The variation in the effective strength of the ILD stack-up as a function of flux type was evaluated using bump shear. Bump shear strength data displayed in Figure 4 shows how the problematic flux 2 correlated with a decreased average force required to shear the bump. Moreover, the greater variance in the flux 2 data suggested an impact of flux on the effective strength of the stack-up, compared to flux 1. Subsequent failure analysis revealed that the sheared bump, for samples not exposed to the problematic flux, fractured primarily at the top metal layers of the die, without much damage to the underlying passivation and ILD layers. The probability of failure through the ILD was also generally observed to increase with increased flux 2 exposure time. The increased variance in bump shear strength for flux 2, along with the higher propensity to fail through the ILD

after flux exposure, yielded direct experimental evidence that flux 2 was interacting with the backend stack-up and altering the effective ILD strength.

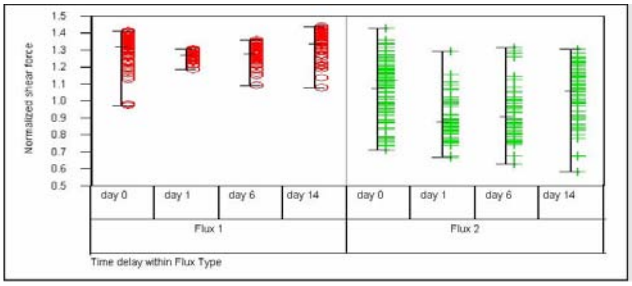

Figure 4: Graph showing the normalized bump shear force for various legs that compare flux type and the number of days of flux exposure

Use of Bump Pull to Understand Impact of HAST on ILD Strength

The following example highlights how a bump pull experiment was used to understand the impact of HAST on the effective backend ILD strength while various FAB backend process parameters are modulated.

Samples for this study were bare dies subjected to various FAB backend processes. Bump pull tests were conducted following exposure to a HAST condition of 130°C and 85% RH for 50 hours. Control units from the same FAB lots with no HAST exposure were included in the study.

Figure 5 shows the bump pull data as a function of three FAB backend processes. The data on control units are consistent for all three experimental legs suggesting good repeatability using bump pull. However, the standard deviation of the signal is fairly large, implying that inherent silicon backend strength varies within a wafer and FAB process. The other aspect of the data corresponds to the pull measurements post 50 hour exposure to 130°C/85 HAST condition for all three FAB processes. In all three experimental legs there is a reduction in the mean pull force from a 20-30% reduction for FAB 1 and three processes to a significant reduction of 80-90% for the FAB 2 process. Physical analysis indicated that the bump pull in the control sample always led to cohesive damage in the passivation layer. However, in the HAST exposed samples, the failure locus changed to being completely at the passivation to UBM interface, leaving a clean passivation layer on the sample, as shown in Figure 6. This was certainly true in the FAB 2 process leg which indicated that HAST exposure was degrading the passivation layer to UBM interfacial strength and making that the weakest interface in the stack-up. The data set pointed to the FAB 2 process leading to a more compromised stack-up compared to the other legs, although all three legs showed some reduction in the pull force to failure.

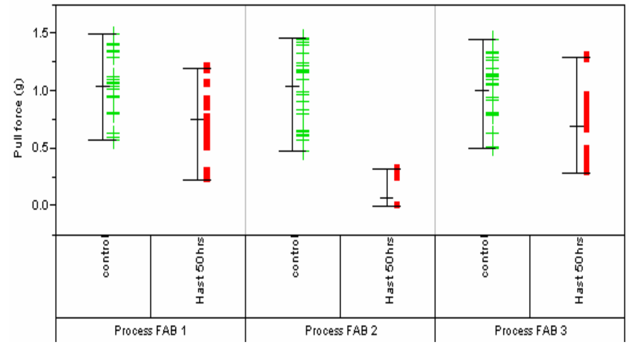

Figure 5: Use of bump pull to understand the impact of HAST reliability test on different FAB backend processes

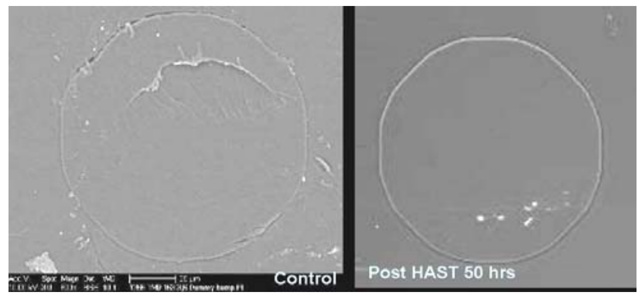

Figure 6: Scanning electron micrographs of residual bump surface after pulling the C4 joints from the die. The left image is of a control unit that indicates some cohesive damage in the passivation layer. The right image is of a sample post HAST exposure.

Case Study Conclusions

The application of bump pull and shear metrologies to understand the effective backend strength of silicon were discussed. The bump pull test applies tensile stress on the silicon backend exposing the weakest interface in the stack-up, while shear applies a mixed mode stress (combination of shear and tensile-compressive stress) and therefore does not guarantee failure of the weakest interface. Two case studies on the application of these metrologies were discussed, showcasing the potential to quantify the variation of silicon backend strength as a function of assembly variables and reliability stresses. These metrologies are also used as "quick turn" process health monitors to provide process engineers a very powerful tool to optimize the process parameters.

CASE STUDY 2: UNDERSTANDING SOLDER JOINT RELIABILITY IN MOBILE SYSTEMS

As previously discussed, the trend toward increased personal mobility has lead to more frequent dropping of computer devices. This is driving the electronics industry

to develop more robust system designs and methods to characterize them.

The mere complexity of mobile systems hampers the understanding of their shock behavior. The systems have chassis that are flexible with massive multiple components (batteries, optical drives, etc.) that react and interact individually or as a group. In addition, the drop height, system orientation at impact, and the surface on which the system is dropped are all variables that add to the complexity. Further, the change to lead-free solder and the reduction in interconnect pitch described previously, add to the challenge of understanding the shock behavior of these devices.

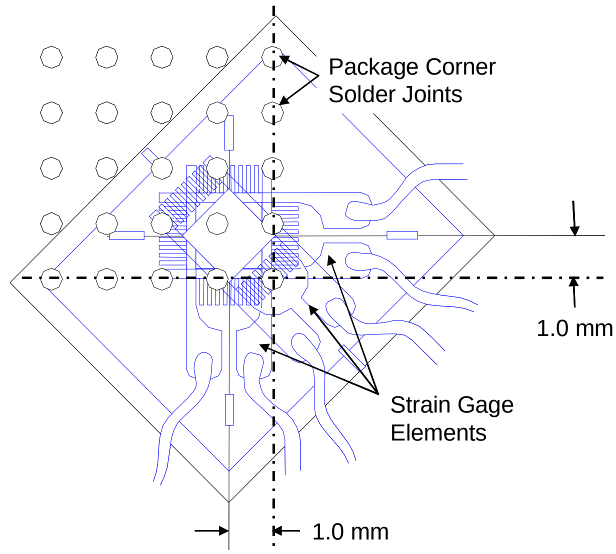

Figure 7: Details of the strain gage placed at the package corner

In order to meet these challenges, new metrologies are needed to measure loads imposed at the component level within the very limited space available inside a laptop or hand-held device. One technique that has been effective within these constrained areas makes use of strain gages. A strain gage is a simple device consisting of a serpentine structure that is etched into a metal foil using photolithography processes. The electrical resistance of this structure will change as the structure is deformed mechanically. Multiple similar structures can be stacked on top of one another to give the deformation in multiple directions at a single location. An example of three stacked strain gages is shown in Figure 7; it is called a rosette. When a circuit board is flexed the strain gages can measure the board surface strain that is related to the curvature of the board [3].

By placing the strain gages at the package corner, directly beneath the corner-most solder joint, one can indirectly determine the loading on the solder joint. At present, there are no means available to directly measure the stress in the solder joint. Therefore, a finite element model is used to correlate the strain in the board (as measured by the strain gage) to the stress in the solder joint. Figure 8 shows this relationship. The board strain has a simple linear relationship to solder ball stress under moderate board strain levels. This relationship also does not change as the package size is reduced.

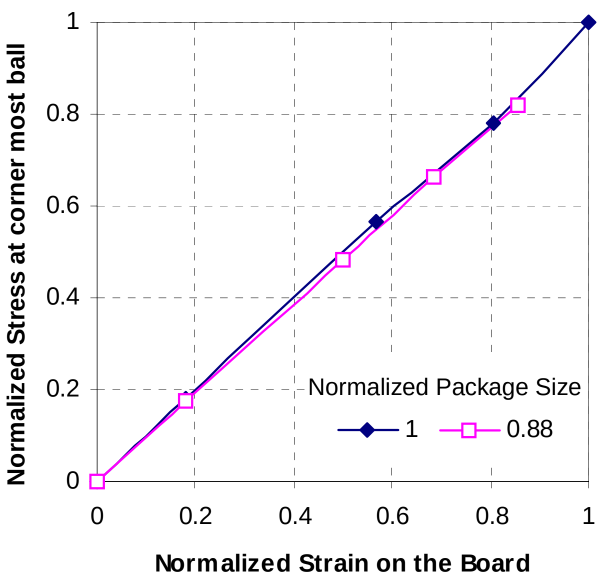

Figure 8: Correlation of the board strain to the stress in the solder joint

Characterizing System Requirements

As board strain has been shown to correlate to the joint stress, we can now use board strain as a metric to characterize the effect of component solder joints when a system is dropped. There is not a common system layout in the mobile laptop market but an example is shown in Figure 9 highlighting key design features. By testing many systems in the same market segment, one can understand the environment to which the component will be subjected. The following case examines the effect of drop shock on the memory controller hub. Six OEM systems were selected and instrumented with strain gages for shock testing. All of the systems were tested to a common input (163g acceleration, ½ sine wave for 2 milliseconds). The shock input is to represent a customer use condition of dropping a laptop approximately eight inches onto a hard surface.

Each system was dropped multiple times and in various orientations. The maximum strain, natural frequency, and bend mode were captured during each drop. These data help establish the customer system "demand" for memory controller hubs in mobile systems. In the following section, we tie the customer system demand to the component capability to assess if there is adequate solder joint capability.

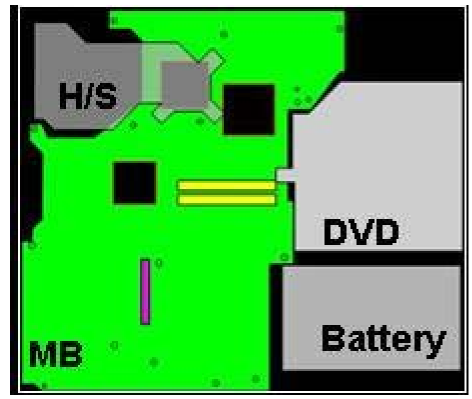

Figure 9: Typical laptop system layout

Characterizing Package Strength

In order to define a package design minimum, one has to test the components at the simplest possible level. To simulate a simplistic but realistic system environment, a Shock Test Board (STB) was developed. Figure 10 shows an example of an STB. This board features a radial hole pattern to allow the board to be attached to the test fixture in multiple configurations to simulate a system board described in the previous section. A single component is placed in the center of the test board. Simple block masses can also be placed on the board to further enhance the response to match the setup to system level tests.

A study was conducted to find the board setup that best matched the response of a typical laptop. Figure 10 shows the setup that best matched mobile systems in terms of strain amplitude, natural frequency, and system mode shape.

In order to determine the ultimate strain-to-failure of a component, a board is tested at increasing strain levels until electrical failure is detected. A small number of additional boards are then tested below this strain level in order to determine the highest board strain that would not cause electrical failure. Once identified, a statistically significant number of sample boards are used at lower test levels to establish a point where the board strain is safe. This strain defines the recommended design maximum for systems.

Figure 10: Shock test board used to test the component capability

The STB provides a means of testing components in a fixed configuration. A designed experiment was conducted to understand the trends of component capability with respect to key design variables such as package size, system board thickness, and solder joint (ball) pitch [4]. This study highlighted many important considerations for system design and understanding of future issues in solder joint reliability. First, the package size does not significantly change the board strain at failure; however, in terms of the shock input, larger packages fail at lower input levels. Second, for increasing board thickness, the shock input required for failure increases while the strain at failure decreases. It is obvious that a thick board requires greater force to bend, leading to the increase in shock acceleration. The reduction in board failure strain is likely due to the increase in solder joint stress with a stiffer board, although there is some speculation that this could also be due to rate sensitivity of the solder and the higher resonant frequency of the board. Last, the trend towards reduced ball pitch will lead to reduced shock performance. While this trend is intuitive, the shock test board gives a means of quantifying the reduction in performance. Figure 11 illustrates this point.

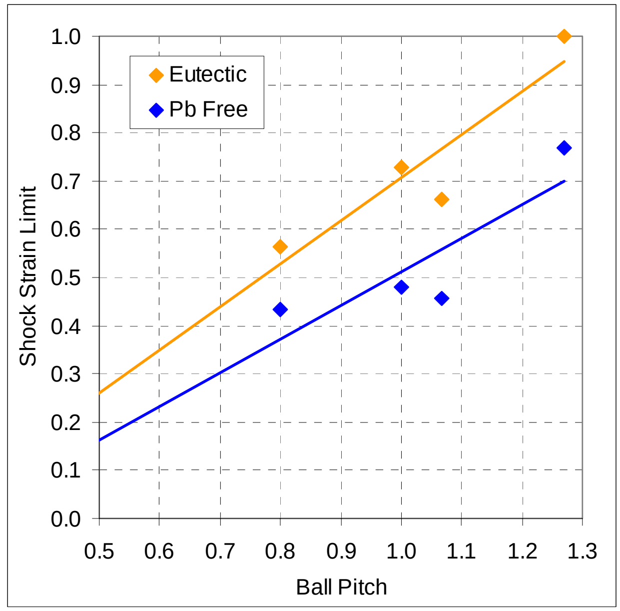

Figure 11: Trend in component capability with ball pitch

VALIDATION–BRINGING BOTH SIDES TOGETHER

These methods give us a critical understanding of the strain produced by representative mobile systems and the capability of an individual component. With these two elements one can now make a direct comparison to assess the risk of component adoption in this market relative to shock impact. Figure 12 shows the comparison of multiple mobile systems with the recommended design maximum. As you sill see, the risk of shock failure for this component is low. This assessment was later confirmed by the successful launch of this lead-free component in mobile systems world-wide.

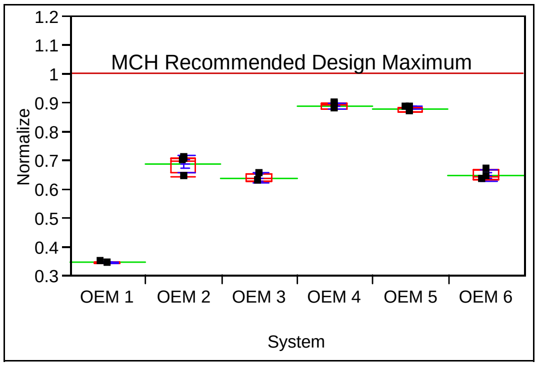

Figure 12: Five Tier 1 Mobility OEM laptops shocked to common input and their recorded board microstrain normalized to Intel recommended package design recommendations

CASE STUDY 3: SAC OPTIMIZATION

The third case examines how to improve Solder Joint Reliability (SJR). SJR performance is governed by two properties: the Bulk property of solder itself and the property of the Interface formed between the solder and base metal or pad. This case study highlights SAC material technology advancements to optimize both Bulk and Interface properties to improve shock performance.

Bulk Optimization–Reducing Joint Stress

The strain rate experienced by solder joints or the boards during drop/shock testing is estimated to be ~10^2/sec., which belongs to dynamic-to-impact loading conditions. Under these conditions, the behavior of the metallic materials is dominated by elasticity. In other words, plasticity is suppressed under these high strain rates. Therefore, elastic compliance is becoming a key material property for shock performance. A high-compliance solder is expected to be favorable for shock performance because it tends to lower stress transferred to vulnerable joint regions (see Figure 13).

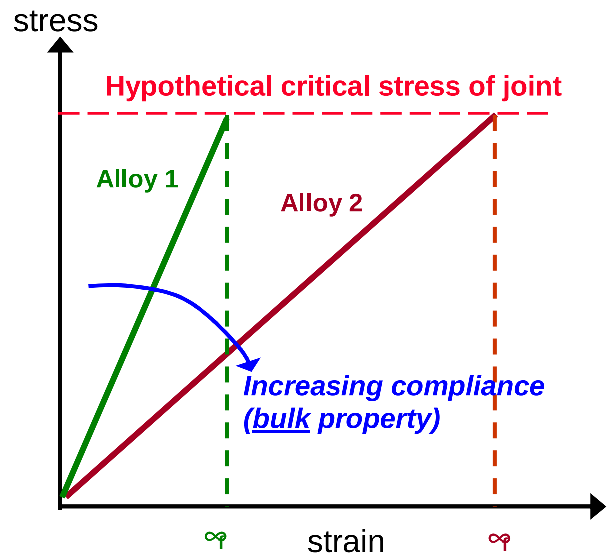

Figure 13: Schematic stress-strain behavior of solder joint with two hypothetical alloys with different compliances. Note high-compliance alloy (Alloy 2) has lower stress under the same board displacement (or strain)

Since compliance is not very sensitive to microstructure, the constituent phase needs to be optimized for higher bulk compliance. Among all constituent phases in SAC, the primary Sn phase has the highest compliance and therefore needs to be optimized. There are two alloying elements in SAC: Ag and Cu. Interfacial reaction and resultant interface characteristics especially on Ni are known to be very sensitive to Cu content [5]. Ag, which does not participate in interfacial reactions, is therefore selected for bulk optimization. Figure 14 is the Sn-rich region of the ternary phase diagram. The variation of Ag content is indicated as a vertical line since Cu content is fixed at this stage. The tie line is constructed for each Ag content along this vertical line, and the relative fraction of the primary Sn phase can be estimated. As indicated in Figure 14, the lower Ag content gives rise to a more primary Sn phase and therefore is expected to result in higher compliance.

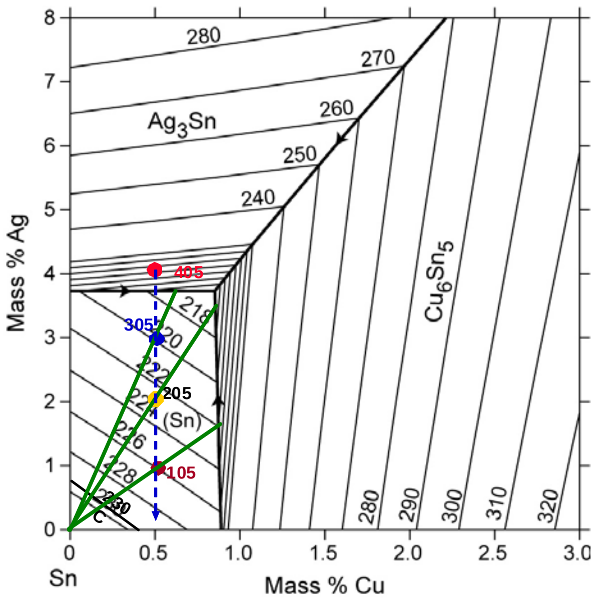

Figure 14: Sn-rich region of Sn-Ag-Cu ternary phase diagram. Variation of Ag content (with fixed Cu content of 0.5%) is indicated by vertical line. The tie line is also shown for representative SAC alloys. Sn-rich phase diagram is taken from. [6]

Thermodynamic simulation of equilibrium solidification shows the comparison between the solidification sequence in SAC305 and 105 (Figure 15). As expected, low Ag alloy such as SAC105 has a higher content of primary Sn phase than SAC305 (~35% vs. 10%).

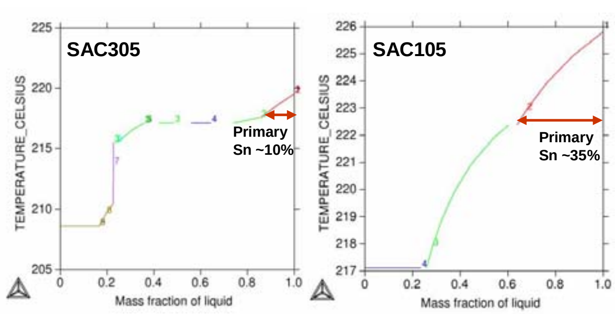

Figure 15: Equilibrium solidification simulation of SAC305 and 105. Note that primary Sn weight fraction is ~15% and ~35% for SAC305 and 105, respectively. Simulation is conducted using Therm-Calc by Thermo-Calc Software, AB with NSLD2 Solder Database.

A series of SAC alloys with different Ag contents was prepared and the elastic moduli of these alloys were measured using ultrasonic stress wave propagation methods. As expected, lowering Ag content progressively reduces the elastic modulus and therefore increases compliance (Table 1). SAC105, for example, has an elastic modulus that is 11% lower than SAC405 (although an elastic modulus of SAC105 is still 17% higher than SnPb). The current data analysis along with other property/performance data suggests that an optimum Ag content is around 1 wt.%.

Table 1: Elastic modulus measured by ultrasonic stress wave propagation technique for SnPb and various SAC alloys

Alloy	SAC405	305	105	SnPb
E [GPa]	53.3	51.0	47.0	40.2

Interface Optimization–Improving Strength

Interfacial reaction of solder is highly dependent on a base metal and therefore any interface optimization should be conducted specific to the surface finish under consideration. Interfacial reaction between the SAC solder and Cu board/substrate pad, for example, leads to two types of Intermetallic Compounds (IMC): scallop-shaped Cu6Sn5 next to solder and planar Cu3Sn next to Cu (note Cu3Sn is not amenable to observation without aging or multiple reflow). It has been observed that interfacial strength or joint integrity inversely scales with the overall thickness of IMC layers on Cu base metal. It has been also suggested that Cu3Sn is particularly more vulnerable to shock fracture than Cu6Sn5. Therefore, optimum interface strength can be achieved on Cu by having a thin overall IMC layer with a minimum Cu3Sn layer.

IMC growth is mostly known to be a diffusion-controlled process, and therefore the key to a thinner IMC layer is to slow down the diffusion process that is responsible for IMC growth. IMC growth is a multi-phase and multi-component diffusion scenario and according to diffusion theory, IMC thickness is governed by the interdiffusion coefficient of the IMC phase under consideration. For example, in the case of a single-layer growth, the IMC thickness, neglecting diffusion through adjacent phases and assuming no interdiffusion cross-terms and constant diffusivities, is given by [7]

$$\textit{IMC thickness} \propto D^{inter}_{ii}$$

where D^{inter}_{ii} is the interdiffusion coefficient for the ternary system such as Sn-Ag-Cu (i is, for example, Sn or Cu). Thus, lowering the interdiffusion coefficient of the IMC under consideration can directly slow down IMC growth kinetics and therefore reduce IMC thickness. Interdiffusion coefficient values for all relevant IMCs are not readily available but there is a reasonably good way to estimate their trend. On the binary phase diagram, if adding A to B increases the liquidous of B, then it will also decrease D [8]. In other words, the ideal solute impurity for a thin IMC layer would be one which 1) has relatively large solubility in the IMC under consideration,

and 2) increases the liquidous of IMC with alloying. Based on the binary phase diagram, several candidate solutes are identified. For example, Ni is isomorphous with Cu and the liquidus of Cu is monotonically increasing with alloying with Ni. Furthermore, according to the known isopleth of the Cu3Sn-Ni system (Figure 16), the addition of Ni does indeed increase the liquidus of Cu3Sn IMC. Ni doping is therefore expected to slow down IMC growth kinetics, especially Cu3Sn, resulting in overall thin IMC layers.

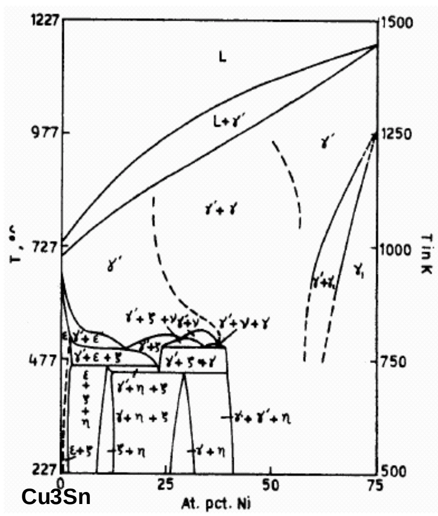

Figure 16: Cu3Sn-Ni Isopleth [9]

Two alloys with low Ag content (~1wt.%) at fixed 0.5 wt.% Cu were prepared with and without Ni doping (<1 wt.%) to examine the effects of impurity doping on interfacial reaction on Cu and resultant joint integrity. Figure 17 shows a SEM cross section of low Ag content alloys with/without Ni doping after solid-state aging. Consistent with thermodynamics and kinetics, while the Cu3Sn layer undergoes significant growth in the alloy without Ni, the same IMC layer is too thin to be resolved in the alloy with NI doping under the same conditions. This reduced IMC thickness and suppressed Cu3Sn layer is indeed found to possess higher interfacial strength favorable for drop performance on a Cu-based surface finish.

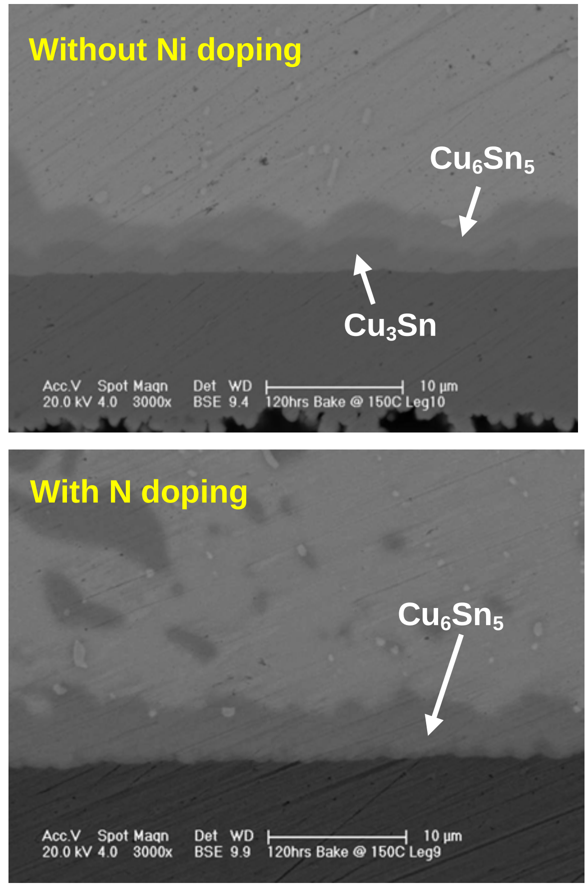

Figure 17: X-section of low Ag (~1 wt.%) alloys with and without Ni doping after 120hr aging at 150°C

In summary, both bulk and interface properties need to be optimized for optimum shock performance. Lowering Ag content for higher compliance is identified as a viable bulk optimization approach. Interface optimization should be conducted specific to the surface finish. On Cu base surface finishes, for example, selected impurity doping is shown to slow down IMC growth kinetics and lead to higher interfacial strength.

CONCLUSION

As illustrated by these case studies, an understanding of reliability issues can be greatly enhanced by focusing the development effort on quantifying the stress imposed and the strength of the material. This approach also leads to results that are more easily extrapolated toward future developments and can yield results even for complex problems. It also leads to reduced development costs and time by reducing or eliminating the need to build and test, as was conventionally done.

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